

1017 U.S. PTO  
10/083402  
02/27/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Yutaka SHIMADA et al.

Appln. No.:

Filed: HERewith

For: MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATED  
CIRCUIT DEVICE

\* \* \*

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any  
assertion as to materiality or prior art effect, the  
documents listed on the attached Form PTO-1449 are hereby  
cited.

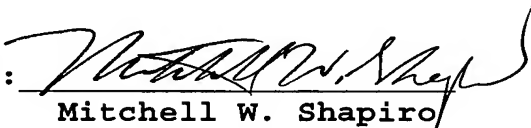
The documents on the attached List are cited in the  
specification, on pages 2-4, and their relevance is  
indicated therein.

Respectfully submitted,

MWS:sjk

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By:

  
Mitchell W. Shapiro  
Reg. No. 31,568

February 27, 2002